In the Claims:

Please amend the above-identified application as follows:

Claim 1 (original) A method of designing logical circuits, comprising the steps of:

a. representing the logic of a logical circuit to be designed as points and vectors in a vector space; and

b. using the points and vectors in a vector space to simplify the logic of the logical circuit to a simpler form; and

c. designing the logical circuit using the simpler form.

Claim 2 (original) A method of manufacturing logical circuits, comprising the steps of:

a. representing the logic of a logical circuit to be manufactured as points and vectors in a vector space; and

b. using the points and vectors in a vector space to simplify the logic of the logical circuit to a simpler form; and

c. using the simpler form to implement the logical circuit in hardware.

Claim 3 (original) A method of simplifying logical circuits, comprising the steps of:

a. representing the logic of a logical circuit as points and vectors in a vector space; and

b. modifying the representation in vector space using at least one process rule of a set of process rules to simplify the logic.

Claim 4 (currently amended) The method of claim 3 in which at least one process rule of a set of process rules consisting of one of the following process rules:

a. Process Rule 1--

a1. Represent ~~the~~in alternational normal schema, the target schema **t**, as a set of vectors in the ANS-space,

a2. Each clause or disjunct of **t** is a position vector (i.e. one pointing to **O**) with **O** at one corner of a set of parallelograms made of propositional addresses to the **í**-point at the other,

a3. Any two other outside vertices of such a parallelogram are implicants which are among the original clauses of **t**;

b. Process Rule 2--

b1. Pick any two clauses,

b2. If there is a propositional address σ at the midpoint between the component clauses, the vector from **í** to σ, ~~i.e. σ,~~ is the simplification of and can replace the relevant clauses of **t**~~, as in the case where t is pq v pq, í is pp and σ is p~~;

c. Process Rule 3--

c1. Generate ί-implicants until each clause or vector has been used at least once,

c2. If a disjunct **d** of **t** cannot be used because it forms no propositional address with any other disjunct, then **d** must appear unmodified in the final schema which is the simplification of **t**;

d. Process Rule 4--

d1. If an ί-point exists in **t**, delete the vectors which produce it in favor of the vector from ί to **O**;

e. Process Rule 5--

e1. For a clause in a schema which subsumes another clause eliminate the subsuming clause;

f. Process Rule 6--

f1. Couples such as **pq v** $\bar{p}\,\bar{q}$ or $\bar{p}\,\bar{q}$**s v pq**$\bar{s}$ cannot be summed to zero~~,~~ at the origin~~.~~;

g. Process Rule 7--

g1. Translate vectors ~~as in Figure 14~~ if a corresponding σ-point exists for an ί-point then ~~6~~ σ is the simplification of ί~~.~~,

g2. Any superpositions of parallel arrows in opposite directions represent equivalences,

g3. For equivalences, (a) ~~Đ~~drop the longer clause at either end of any double-headed arrow, (b) ~~Đ~~drop pairs, triples etc. of double-headed arrows which meet at a point in favor of the vector from that point to **O** and (c) ~~Đ~~drop a vector or clause in the target schema which is itself the resultant of any other two vectors;

h. Process rule 8--

h1. A simplification is complete if in the system which replaces the target schema no vectors or clauses are subsumed by others and no double-headed vectors remain ~~(i.e. if all equivalences in the system have been exploited)~~.

Claim 5 (original) Apparatus for simplifying logical circuits, comprising:

a. a processing element configured to represent the logic of a logical circuit to be simplified as points and vectors in a vector space and to use the points and vectors to simplify the logic of the logical circuit to a simpler form.

Claim 6 (original) The apparatus of claim 5 in which the processing element is an optical computer.

Claim 7 (original) The apparatus of claim 5 in which the processing element is a digital computer.

Claim 8 (original) The apparatus of claim 1 in which the processing element is an colorimetric computer.

Claim 9 (original) The apparatus of claim 1 in which the processing element is an analog computer.

Claim 10 (original) A computer program product, comprising:

a. a memory element; and

b. a computer program stored on said memory medium, said computer program comprising instructions for representing the logic of a logical circuit to be designed as points and vectors in a vector space and for using the points and vectors in a vector space to simplify the logic of the logical circuit to a simpler form and for designing the logical circuit using the simpler form.

Claim 11 (original) A computer program product, comprising:

a. a memory element; and

b. a computer program stored on said memory medium, said computer program comprising instructions for representing the logic of a logical circuit to be manufactured as points and vectors in a vector space, and for using the points and vectors in a vector space to simplify the logic of the logical circuit to a

simpler form, and for using the simpler form to implement the logical circuit in hardware.

Claim 12 (original) A computer program product, comprising:

a. a memory element; and

b. a computer program stored on said memory medium, said computer program comprising instructions for representing the logic of a logical circuit as points and vectors in a vector space, and for modifying the representation in a vector space using at least one process rule of a set of process rules to simplify the logic.

REMARKS

Claims 1-12 remain in the application. Claims 1-12 stand rejected. Applicants appreciate the Examiner's detailed review of the application which revealed a disconnect between the claims filed in the November 8, 2004, response and the claims the Examiner held to be pending in the application.

In the office action, the Examiner has indicated that a complete response should include:

1. an amendment to the claims, see Exhibit A, that brings them into alignment with claims in Exhibit B, with amendments clean up any informalities.
2. amendments that resolve the use of indefinite language of "such as" and the use of "i.e."
3. include the amendments to the Abstract and specification as provided in the after final amendments dated June 29, 2005.
4. providing a copy of the references cited in the Applicant's specification so that the Examiner may determine if they are essential or material to the case. This is not a formal requirement under 37 C.F.R. 1.105, however, not providing these materials may precipitate one.

The claims have been amended to bring them into alignment with those presented on November 8, 2004. The amendments have been reviewed to remove any possible and indefinite language and to clean up any informalities.

The amendments to the Abstract and specification that were provided in the amendment dated June 29, 2005, have been included in the amendments submitted herewith.

Applicant respectfully requests reconsideration of the suggestion by the Examiner that copies of the references cited in the specification should be submitted so that the Examiner may determine if they are essential or material to the case. The Examiner graciously noted that this is not a formal requirement at this time, but might later become one.

The Examiner could correctly determine the references to be essential if in fact there were something missing from the enablement or best mode of the specification that would possibly be filled in by providing copies of those references. However, the Examiner has not identified any insufficiency in the specification and therefore there is nothing with respect to which the articles could be considered essential. For the record, the Quine reference in the specification is a textbook having over 500 pages. The utility of providing that source to the Examiner would be burdensome and difficult, especially when there is no identified need for providing copies of the documents. That a reference to an article or a source outside of the specification might possibly contain something that would indicate that the specification lack essential material does not seem to be a reasonable basis for making a requirement for information. Accordingly, applicant respectfully request that the Examiner reconsider that requirement.

In re Patent Application of:
WESTPHAL
Serial No. **09/787,290**
Filed: **MARCH 15, 2001**

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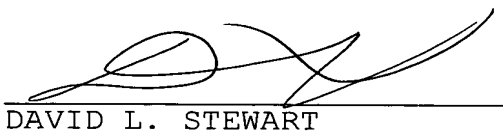
In as much as applicants have responded to each of the requirements of the Examiner and have provided the set of claims that corresponds to those submitted on November 8, 2004, applicant respectfully request that the Examiner withdraw any outstanding rejections and allow the application to issue as a patent.

Please charge any shortage in fees due in connection with the filing of this paper, including Extension of Time fees, to Deposit Account No. 01-0484 and please credit any excess fees to such deposit account.

Respectfully submitted,



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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: MAIL STOP AMENDMENT, COMMISSIONER OF PATENTS, P.O. BOX 1450, ALEXANDRIA, VA 22313-1450, on this 9th day of September, 2005.